Docket No. 03-0290

PATENT

Certificate of Mailing by "Express Mail"

Mailing Label Number EV335604380US

Date of Deposit: August 26, 2003

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office Box Addressee" service under 35 CFR 1.10 on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

James R. Foley, Reg. No. 39,979

SHARING FUSE BLOCKS BETWEEN MEMORIES IN HARD-BISR

Inventors

Mukesh K. Puri
44978 Lynx Drive
Fremont, CA 94539

Ghasi R. Agrawal
1633 Canary Drive
Sunnyvale CA 94087

Background of the Invention

The present invention generally relates to Built-in-Self-Repair (BISR) schemes, and more specifically relates to memories and fuse blocks.

Built-in-Self-Repair (BISR) is a scheme wherein a certain amount of redundant elements are provided in each memory so that random process defects do not cause excessive yield loss. The current versions of BISR run different patterns at wafer-level to test the memories on the chip and generate a repair solution which can be scanned out of the chip and written to an output file. The repair solutions are then programmed on the respective devices by blowing fuses. In the system, a power-on state machine loads the fuse values into the memories. This repairs the memories (i.e., soft-repair) after which they can be accessed in the functional mode.

Figure 1 illustrates the structure of a hard-BISR scheme which is currently in use, while Figure 2 illustrates the method steps of its usage. The scheme provides that memories 30 ("Mem-1", "Mem-2", . . . "Mem-100") are provided on a core 32 which is on a chip 34, and provides that fuse blocks 36 ("Bl-1", "Bl-2", . . . "Bl-100") are provided on the chip 34 and are connected to the memories 30 via routing 38. The scheme provides that there is one fuse block for each repairable memory instance (i.e., fuse block "Bl-1" is routed to memory "Mem-1", fuse block "Bl-2" is routed to memory "Mem-2", . . . fuse block "Bl-100" is routed to memory "Mem-100"). Figure 1 shows the specific example where there are 100 memories and 100

fuse blocks. Each of the fuse blocks contains a number of fuses which can be blown to program the repair solution for each memory. The size of these blocks is a function of the amount of redundancy available. For example, a given memory instance with 4 redundant rows needs about 52 fuses and would be (48u x 287u) in size. However, these fuse blocks are an overhead in terms of Silicon area utilization and can cause complications in layout and routability of the design. Moreover, in the majority of repairable devices, only a few of the memory instances actually need repair. Therefore, the bulk of the fuse blocks are left unused.

Objects and Summary of the Invention

An object of am embodiment of the present invention is to provide a BISR scheme which provides that fuse blocks are shared between memories to reduce hard-BISR implementation costs.

Another object of am embodiment of the present invention is to provide a BISR scheme which saves Silicon area and reduced complications in routing and layout.

Briefly, and in accordance with at least one of the foregoing objects, an embodiment of the present invention provides a BISR scheme which includes a plurality of memories serially connected to a fuse controller. A plurality of fuse blocks are also serially connected to the fuse controller. There are more memory instances than there are fuse blocks, and the fuse controller is configured to allow the fuse blocks to be shared between memories to reduce hard-BISR implementation costs. Preferably, each fuse block includes fuse elements which can be programmed with the memory instance number which needs to be repaired. The fuse block reduces routing congestion and is preferably configured to provide the flexibility of assigning any fuse block to any instance that needs repair. The programmable fuse elements are preferably loaded into a counter (which is preferably a part of the fuse controller) which ensures that the correct block information gets loaded into the corresponding memory instance.

Brief Description of the Drawings:

The organization and manner of the structure and operation of the invention, together with further objects and advantages thereof, may best be understood by reference to the following description, taken in connection with the accompanying drawing, wherein:

Figure 1illustrates the structure of a prior art BISR scheme;

Figure 2 illustrates usage of the prior art BISR scheme shown in Figure 1;

Figure 3 illustrates the structure of a BISR scheme which is in accordance with an embodiment of the present invention; and

Figure 4 illustrates usage of the BISR scheme shown in Figure 3.

Description

While the invention may be susceptible to embodiment in different forms, there is shown in the drawings, and herein will be described in detail, a specific embodiment with the understanding that the present disclosure is to be considered an exemplification of the principles of the invention, and is not intended to limit the invention to that as illustrated and described herein.

Figure 3 illustrates the structure of a BISR scheme which is in accordance with an embodiment of the present invention, and Figure 4 illustrates its usage. The scheme provides that fuse blocks 50 ("Bl-1", "Bl-2", . . . "Bl-10") are shared between memories 52 ("Mem-1", "Mem-2", . . . "Mem-100") to reduce hard-BISR implementation costs. The scheme saves Silicon area and reduced complications in routing and layout.

The scheme includes a plurality of memories 52 ("Mem-1", "Mem-2", . . . "Mem-100") which are serially connected to a fuse controller 54, and a plurality of fuse blocks 50 ("Bl-1", "Bl-2", . . . "Bl-10") are also serially connected to the fuse controller. There are more memory instances (a quantity of 100 in Figure 3) than there are fuse blocks (a quantity of ten in Figure 3), and the fuse controller 54 is configured to allow the fuse blocks 50 to be shared between memories 52. Preferably, each fuse block 50 includes fuse elements which can be programmed with the memory instance number which needs to be repaired. The fuse block

reduces routing congestion and is preferably configured to provide the flexibility of assigning any fuse block to any instance that needs repair. The programmable fuse elements are preferably loaded into a counter (which is preferably a part of the fuse controller 54) which ensures that the correct block information gets loaded into the corresponding memory instance. As such, the fuse controller 54 is configured to regulate the scan-in sequence, and the connection 56 from the fuse controller 54 to the chain of memories 52 provides the routing for fuse information. While the example shown in Figure 3 provides one hundred memories, one fuse controller, and ten fuse blocks, other quantities may be provided depending on the structure and application.

Compared to Figure 1, the individual fuse block size of the scheme shown in Figure 3 can be increased to allow for additional fuse elements which can be programmed with the memory instance number which needs to be repaired. For example, a design with 100 memory instances may have only 10 fuse blocks as per the scheme shown in Figure 3 versus 100 blocks required under the scheme shown in Figure 1. Preferably, each of the fuse blocks has some additional fuse elements (such as 7 in the particular example depicted in Figure 3) to program which memory instance would get loaded from that specific block. As discussed, the fuse blocks are serially connected to all memories through the fuse controller which reduces routing congestion and provides the flexibility of assigning any block to any

instance that needs repair. The additional fuse elements are loaded into a counter (which is preferably part of the fuse controller) which ensures that the correct block information gets loaded into the corresponding memory instance.

Figures 1 and 3 basically show the differences between the currently, widely used BISR scheme and a BISR scheme which is in accordance with an embodiment of the present invention. The notations "Mem-1", "Mem-2", . . . "Mem-100" in these figures indicate the memory instances along with the BIST (Built-In Self-Test) and BISR logic, while "Bl-1", "Bl-2", . . . "Bl-100" (in Figure 1) and "Bl-1", "Bl-2", . . . "Bl-10" (in Figure 3) show the fuse blocks. Again, while Figure 1 shows 100 memories and 100 fuse blocks, and Figure 3 shows 100 memories, one fuse controller, and 10 fuse blocks, other quantities are possible.

While an embodiment of the present invention is shown and described, it is envisioned that those skilled in the art may devise various modifications of the present invention without departing from the spirit and scope of the appended claims.